IN THE CLAIMS:

1. (currently amended) An integrated circuit comprising a set of active devices connected by a set of interconnect structures, in which at least some of the interconnect structures are formed by a conductive material embedded in an interlevel dielectric, the conductive material being separated from the dielectric by at least one liner layer, in which said at least one liner layer is formed from a liner material comprising Tantalum and Nitrogen in an atomic concentration ratio N:Ta > 1.2.

2. (currently amended) An integrated circuit according to claim 1, in which said liner material comprises TaN_x, where X is greater than 1.2.

3. (currently amended) An integrated circuit according to claim 1, in which the thickness of said liner material is less than 5 nm.

4. (currently amended) An integrated circuit according to claim 1, in which the thickness of said liner material is less than 0.75nm.

5. An integrated circuit according to claim 1, in which the thickness of said liner material is less than 0.5 nm.

6. (currently amended) An integrated circuit according to claim 1, in which the resistivity of said liner material is greater than 1000 micro-Ohm-cm.

7. (currently amended) An integrated circuit according to claim 6, in which the thickness of said liner material is less than 0.75 nm.

8. (currently amended) An integrated circuit according to claim 3, in which the resistivity of said liner material is greater than 1000 micro-Ohm-cm.

9. (currently amended) An integrated circuit according to claim 8, in which the thickness of said liner material is less than 0.75 nm.

10. (currently amended) An integrated circuit according to claim 8, in which the thickness of said liner material is less than 0.5 nm.

11. (currently amended) An integrated circuit comprising a set of active devices connected by a set of interconnect structures, in which at least some of the interconnect structures are formed by a conductive material embedded in an interlevel dielectric, the conductive material being separated from the dielectric by at least one liner layer, in which

said at least one liner layer is formed from a liner material comprising TaN_x and having a thickness less than 5nm.

12. (currently amended) An integrated circuit according to claim 11, in which x is greater than 1.2.

13. (currently amended) An integrated circuit according to claim 11, in which said thickness is less than 0.75 nm.

14. An integrated circuit according to claim 11, in which said thickness is less than 0.5 nm.

15. (currently amended) An integrated circuit according to claim 11, in which said liner material has a resistivity greater than 1000 micro-Ohm-cm.

16. (currently amended) An integrated circuit according to claim 12, in which said liner material has a resistivity greater than 1000 micro-Ohm-cm.

17. (currently amended) An integrated circuit according to claim 13, in which said liner material has a resistivity greater than 1000 micro-Ohm-cm.

18. (withdrawn) A method of forming an interconnect structure in an integrated circuit comprising a layer of a conductive material embedded in an interlevel dielectric, the conductive material being separated from the dielectric by at least one liner layer, comprising the steps of introducing Ta and N into a chamber containing an integrated circuit having an aperture formed in a layer of interlevel dielectric, thereby depositing said liner layer, and thereafter depositing a layer of conductive material in said aperture and in which said at least one liner layer is formed from a material comprising TaN_x, where x is greater than 1.2.

19. (withdrawn) A method of forming an interconnect structure according to claim 18, in which said liner layer is deposited with a thickness less than 5nm.

20. (withdrawn) A method of forming an interconnect structure according to claim 18, in which said liner layer is deposited with a thickness less than 0.75 nm.

21. (withdrawn) A method of forming an interconnect structure according to claim 18, in which said liner layer is deposited with a thickness less than 0.5nm.

22. (withdrawn) A method of forming an interconnect structure according to claim 15, in which said liner layer has a resistivity greater than 1000 micro-Ohm-cm.

23. (withdrawn) A method of forming an interconnect structure according to claim 19, in which said liner layer has a resistivity greater than 1000 micro-Ohm-cm.

24. (withdrawn) A method of forming an interconnect structure according to claim 20, in which said liner layer has a resistivity greater than 1000 micro-Ohm-cm.

25. (withdrawn) A method of forming an interconnect structure according to claim 21, in which said liner layer has a resistivity greater than 1000 micro-Ohm-cm.